AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0024] with the following amended paragraph:

[0024] The output of the down-converter mixer 114 is fed to an intermediate frequency (IF) filter 118. The output of the IF filter 118 is fed to a quadrature demodulator 120 which uses the signal from an intermediate frequency phase lock loop (IF PLL) 122 to demodulate the signal into two signals having quadrature phase. Specifically, the quadrature demodulator 120 has a first output 124a and a second output 124b, which present the demodulated signal with a quadrature phase shift. Each of the outputs 124a and 124b are fed to a respective anti-aliasing filter 126a and 126b, as seen in Figure 3. The output of each anti-aliasing filter 126a and 126b is fed to a respective analog to digital converter 128a and 128b. Each of the analog to digital converters 128a and 128b [[are]] is operative to convert the received analog signal into a digital representation. The digital representation of the signal is then fed into the baseband processor [[32]] 108 for decoding, as previously described above. The baseband processor [[32]] 108 will capture the narrowband signal during decoding in order to determine the control information.